



# **STIC Search Report**

**EIC 2800**

**STIC Database Tracking Number: 151836**

**TO: Chandra Chaudhari**  
**Location: JEF-6A49**  
**Art Unit : 2891**  
**Wednesday, April 27, 2005**

**Case Serial Number: 10/692272**

**From: Darcy Bates**  
**Location: EIC 2800**  
**JEF- 4B68**  
**Phone: 571-272-2540**

**darcy.bates@uspto.gov**

## **Search Notes**

**Re: 10/692,272 US 6,475,846**

**Attached are search results.**

**No U. S. litigation was found in searches of  
Lexis-Nexis and Questel-Orbit databases.**

**If more searching or explanation is needed, please let  
me know.**

**Thanks,  
Darcy Bates**



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Patent Search - Number: 6,475,846



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444182 (08) 6475846 November 5, 2002

## UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

**6475846**♦ [Get Drawing Sheet 1 of 6](#)[Access PDF of Official Patent](#) \*[Check for Patent Family Report PDF availability](#) \*

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November 5, 2002

Method of making floating-gate memory-cell array with digital logic transistors

**REISSUE:** October 22, 2003 - Reissue Application filed Ex. Gp.: 2813; Re. S.N. 10/692,272 (O.G. March 23, 2004)

**INVENTOR:** Marotta, Giulio - Contigliano, Italy (IT); Santin, Giovanni - S. Rufina, Italy (IT); Smayling, Michael C. - Missouri City, Texas; Matsuoka, Misako A. - Plano, Texas; Fukawa, Satoru - Ibaraki-ken, Japan (JP)

**APPL-NO:** 444182 (08)**FILED-DATE:** May 18, 1995**GRANTED-DATE:** November 5, 2002**ASSIGNEE-AT-ISSUE:** Texas Instruments Incorporated, Dallas, Texas, 02

**ASSIGNEE-AFTER-ISSUE:** May 18, 1995 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., TEXAS INSTRUMENTS INCORPORATED POST OFFICE BOX 655474, M/S 219 DALLAS TEXAS 75265, Reel and Frame Number: 07726/0724  
July 10, 1995 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., TEXAS INSTRUMENTS INCORPORATED POST OFFICE BOX 655474 M/S 219 DALLAS TEXAS 75265, Reel and Frame Number: 07726/0701

**LEGAL-REP:** Brady, W. James; Telecky, Jr., Frederick J. - ##0

**PUB-TYPE:** November 5, 2002 - Utility Patent having no previously published pre-grant publication (B1)

**PUB-COUNTRY:** United States (US)**US-MAIN-CL:** 438#201**US-ADDL-CL:** 257#E21.689, 257#E27.081, 438#258, 438#275**CL:** 438, 257, 438

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patno=6475846

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<a href="#">and</a>	and
<a href="#">or</a>	or
<a href="#">w/N</a>	within N words
<a href="#">not w/N</a>	not within N words
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<a href="#">w/p</a>	in same paragraph
<a href="#">not w/p</a>	not in same paragraph
<a href="#">w/seg</a>	in same segment
<a href="#">not w/seg</a>	not in same segment
<a href="#">w/s</a>	in same sentence
<a href="#">not w/s</a>	not in same sentence
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Query/Command : us6475846/pn

\*\* SS 3: Results 1

Search statement 4

Query/Command : prt fu legalall max

1 / 1 PLUSPAT - @QUESTEL-ORBIT - image  
PN - US6475846 B1 20021105 [US6475846]  
TI - (B1) Method of making floating-gate memory-cell array with digital  
logic transistors  
PA - (B1) TEXAS INSTRUMENTS INC (US)  
PAO - Texas Instruments Incorporated, Dallas TX [US]  
IN - (B1) MAROTTA GIULIO (IT); SANTIN GIOVANNI (IT); FUKAWA SATORU  
(JP); MATSUOKA MISAKO A (US); SMAYLING MICHAEL C (US)  
AP - US44418295 19950518 [1995US-0444182]  
PR - US44418295 19950518 [1995US-0444182]  
IC - (B1) H01L-021/8238  
EC - H01L-021/8247M2P2  
H01L-027/105  
PCL - ORIGINAL (O) : 438201000; CROSS-REFERENCE (X) : 257E21689  
257E27081 438258000 438275000  
DT - Corresponding document  
CT - US5047358; US5225700; US5411908  
STG - (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001  
AB - A nonvolatile memory array is encased in a P-well, and the P-well  
encased in a deep N-well, the two wells separating the memory  
array from the integrated circuit substrate and from the other  
circuitry of the integrated circuit. At the same time the deep  
N-well is formed for the nonvolatile memory array, deep N-wells  
are formed for the high-voltage P-channel transistors of the logic  
circuitry. At the same time the P-well is formed for the  
nonvolatile memory array, P-wells are formed for the low-voltage  
N-channel transistors. The memory array contains nonvolatile cells  
of the type used in ultra-violet-erasable EPROMs. During erasure,  
the isolated-well formation allows the source, the drain and the  
channel of selected cells to be driven to a positive voltage. The  
isolated well is also driven to a positive voltage equal to, or  
slightly greater than, the positive voltage applied to the source  
and drain, thus eliminating the field-plate breakdown-voltage  
problem.  
UP - 2002-46

1 / 1 LGST - @EPO  
PN - US6475846 B1 20021105 [US6475846]  
AP - US44418295 19950518 [1995US-0444182]  
ACT - 20040323 US/RF-A  
REISSUE APPLICATION FILED  
EFFECTIVE DATE: 20031022  
UP - 2004-14

4/27/05

US 6,475,846

10/692272

1 / 1 CRXX - ©CLAIMS/RRX  
AN - 3779602  
PN - 6,475,846 A 20021105 [US6475846]  
PA - Texas Instruments Inc  
PT - C (Chemical)  
ACT - 20031022 REISSUE REQUESTED  
ISSUE DATE OF O.G.: 20040323  
REISSUE REQUEST NUMBER: 10/692272  
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2813

Reissue Patent Number:

UP - 2004-13  
UACT- 2004-03-23

Search statement 4

Query/Command : fam us6475846/pn

1 Patent Groups  
\*\* SS 4: Results 2

Search statement 5

Query/Command : famstate nonstop

1 / 2 PLUSPAT - ©QUESTEL-ORBIT - image  
PN - US6475846 B1 20021105 [US6475846]  
STG - (B1) U.S. Patent (no pre-grant pub.) after Jan. 2, 2001  
TI - (B1) Method of making floating-gate memory-cell array with digital  
logic transistors  
PA - (B1) TEXAS INSTRUMENTS INC (US)  
PAO - Texas Instruments Incorporated, Dallas TX [US]  
IN - (B1) MAROTTA GIULIO (IT); SANTIN GIOVANNI (IT); FUKAWA SATORU  
(JP); MATSUOKA MISAKO A (US); SMAYLING MICHAEL C (US)  
IC - (B1) H01L-021/8238  
AP - US44418295 19950518 [1995US-0444182]  
PR - US44418295 19950518 [1995US-0444182]  
EC - H01L-021/8247M2P2  
H01L-027/105  
PCL - ORIGINAL (O) : 438201000; CROSS-REFERENCE (X) : 257E21689  
257E27081 438258000 438275000  
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UP - 2002-46

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PN - US6475846 B1 20021105 [US6475846]  
AP - US44418295 19950518 [1995US-0444182]

4/27/05

US 6,475,846

10/692272

ACTE- 20040323 US/RF-A  
REISSUE APPLICATION FILED  
EFFECTIVE DATE: 20031022  
UP - 2004-14

2 / 2 PLUSPAT - @QUESTEL-ORBIT - image  
PN - US5907171 A 19990525 [US5907171]  
STG - (A) United States patent  
TI - (A) Method of making floating-gate memory-cell array with digital  
logic transistors  
PA - (A) TEXAS INSTRUMENTS INC (US)  
PAO - Texas Instruments Incorporated, Dallas TX [US]  
IN - (A) SANTIN GIOVANI (IT); MAROTTA GIULIO (IT); SMAYLING MICHAEL C  
(US); MATSUOKA MISAKO A (US); FUKAWA SATORU (JP)  
IC - (A) H01L-029/788  
AP - US97836397 19971125 [1997US-0978363]  
PR - US97836397 19971125 [1997US-0978363]  
US44418295 19950518 [1995US-0444182]  
EC - H01L-021/8247M2P2  
H01L-027/105  
PCL - ORIGINAL (O) : 257315000; CROSS-REFERENCE (X) : 257E21689  
257E27081 257316000  
DT - Basic



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<u>and not</u>	and not

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